HIGHLY INTEGRATED THREE-DIMENSIONAL MMIC SINGLE-CHIP RECEIVER AND TRANSMITTER

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ABSTRACT

A three-dimensional (3D) MMIC structure with thin polyimide-film layers on wafers significantly increases the integration level of MMICs. We newly developed 9.2—12 GHz receiver and 9.5—14 GHz transmitter chips with 20 dB gain using 3D MMIC technology. The integration levels of these chips are nearly three times as high as those of conventional planar ones.

INTRODUCTION

The spread of commercial wireless communication systems has resulted in an increasing demand for highly integrated multifunctional MMICs. Recently, many single-chip MMIC approaches in planar forms for miniaturizing receivers and transmitters have been reported. However, the integration level I, defined as gain (G in dB)-bandwidth ($\Delta f/f_0$) product per mm^2, decreases along a curve of $I \times [f\,(\mathrm{GHz})]^{1/2} = 2$ (I = 0.6 at 10 GHz) because of the considerably limited bandwidth and conversion gain obtained from the small area [1]. We developed 9.2—12 GHz receiver and 9.5—14 GHz transmitter chips with 20 dB gain by using three-dimensional (3D) MMIC technology [2-8] which effectively reduces circuit area due to its stacking effect as well as narrow line-width and spacing. The receiver integrates a 4-stage front-end amplifier, an LO amplifier and an image-rejection mixer in a 2 × 2 mm chip. The transmitter also integrates an IF amplifier with balanced outputs, an LO amplifier, an RF buffer amplifier and a balanced upconverter in a 1.9 × 1.9 mm chip. The integration levels achieved in the X-band in the receiver and transmitter are I = 1.5 and 2.3 respectively. These levels are nearly three times as high as those which have been previously achieved in conventional planar single-chip receivers and transmitters.

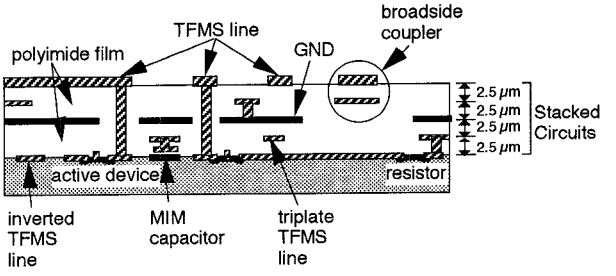

Fig. 1 Basic structure of the 3D MMIC. Ground metal (GND) is located in a middle polyimide layer and passive circuits are stacked up above and below the GND and constructed with narrow TFMS lines and inverted TFMS lines.

THREE-DIMENSIONAL MMIC

Figure 1 shows the basic structure of the 3D MMIC. Active devices, such as FETs, resistors and MIM capacitors are formed on a substrate. Thin polyimide films and conductors are stacked on the substrate, and conductors are connected with through-holes to each other. Each of the polyimide films is 2.5 μm in thickness.

The most significant feature of the structure is that a ground metal is located in the middle of the polyimide layers and passive circuits are stacked up above and below the ground metal and constructed with narrow thin film microstrip (TFMS) lines [2] and inverted TFMS lines with widths of 30 μm at maximum (around 10 μm on average). The 3D MMIC technology effectively reduces the circuit area and significantly increases integration level.

SINGLE-CHIP RECEIVER DESIGN

Figure 2 shows a block diagram of the X-band single-chip receiver MMIC. A 4-stage front-end amplifier which includes a low-noise amplifier and three variable gain amplifiers, an LO amplifier, and an image-rejection mixer are integrated in a single chip. Figure 3 shows a microphotograph of the fabricated X-band single-chip receiver. The chip size is only 2 × 2 mm. The layout was designed on a 3 × 3 matrix of a 0.6 × 0.6 mm space. The measured performance of the single-chip receiver is

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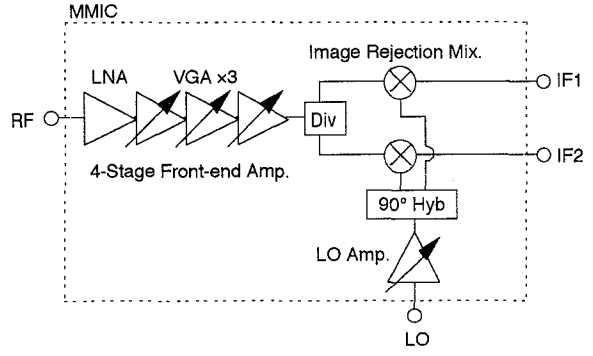


Fig. 2 Block diagram of the proposed 3D MMIC single-chip receiver which includes a low noise amp., three variable gain amps., an LO amp., two unit mixers, a Wilkinson divider and a 90° hybrid.

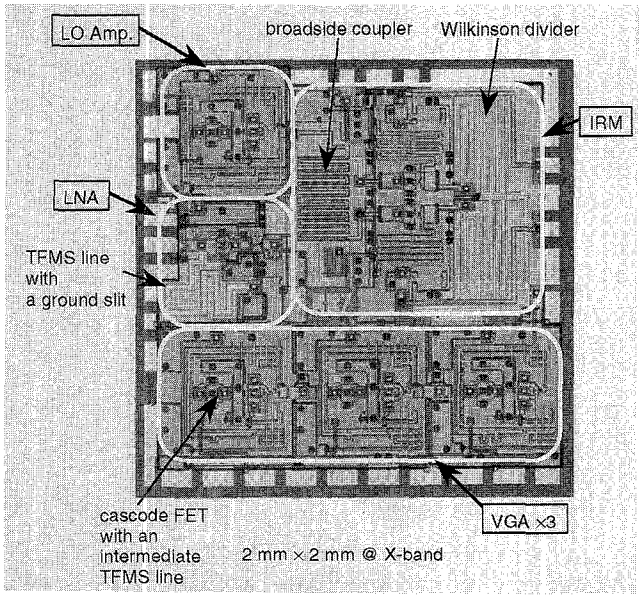
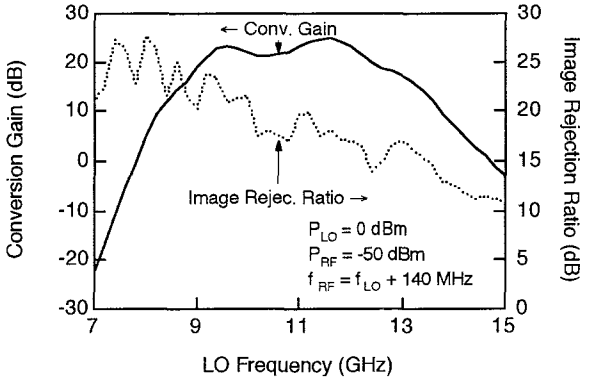


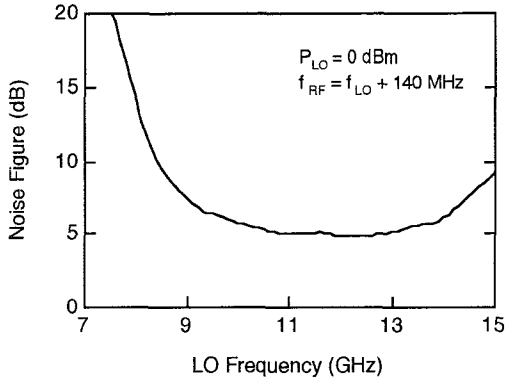
Fig. 3 Microphotograph of the fabricated X-band single-chip receiver. A low-noise amplifier, three variable gain amplifiers, an LO amplifier and an image-rejection mixer constructed with two unit mixers, a Wilkinson divider and a 90° broadside coupler are integrated in a 2 × 2 mm chip.

shown in Fig. 4. A conversion gain of 23 ± 2 dB and image-rejection ratio of better than 15 dB are obtained over the 9.2—12 GHz frequency range with a noise figure of 5.5 ± 0.5 dB and a gain control range of over 50 dB, where LO power is 0 dBm, RF power is −50 dBm, and IF frequency is 140 MHz.

The low-noise amplifier uses a common-source-FET. A TFMS line with a ground slit below the conductor strip is employed in the input matching circuit of the low-noise amplifier to widen the line-width and reduce the noise figure. This line was newly designed for the 3D structure. Figure 5 shows a cross-sectional view and calculated characteristics of the line. The characteristic impedance of 50 Ω can be obtained when w = 30 μm and g = 30 μm. The width of the line is about 1.5 times



(a) Conversion gain and image rejection ratio



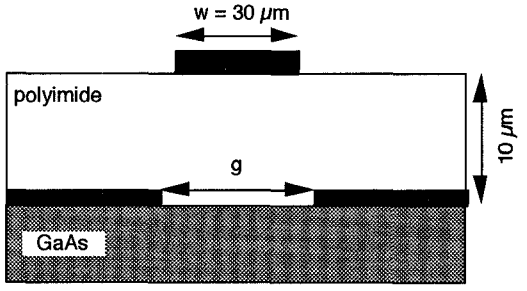
(b) Noise figure

Fig. 4 Measured performance of the fabricated single-chip receiver.

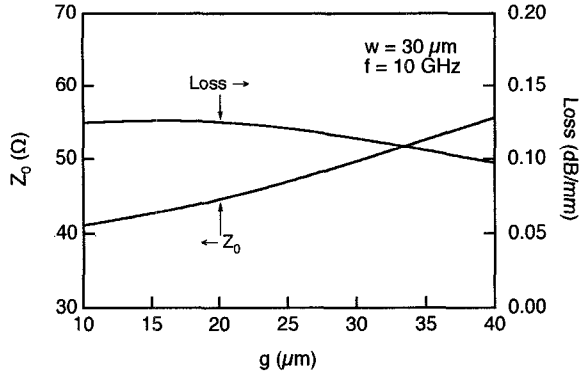
as wide as conventional TFMS line's (22μm), and the loss factor is only 0.11 dB/mm at 10 GHz. The measured gain and noise figure are 6.1 ± 0.9 dB and 4.2 ± 0.8 dB, respectively, from 9.2 to 12 GHz. The noise figure is reduced to nearly 1.5 dB less than that of an amplifier with only conventional TFMS lines for the input matching circuit.

The variable gain amplifier employs a cascode FET which is constructed with a common-source-FET (CSF) and a common-gate-FET (CGF) connected with a nearly 2-mm-long TFMS line to achieve a higher matching gain. Gain control is achieved by adjusting the second-FET gate bias voltage. The capacitive coupling-effect between FET electrodes and the ground metal above the FETs is considered in the amplifier design. The measured gain and noise figure are 8.2 ± 0.4 dB and 5.3 ± 0.3 dB, respectively, from 9.2 to 12 GHz. The saturation power is greater than 10 dBm. The variable gain amplifier is also used as an LO amplifier.

The image-rejection mixer is constructed with a Wilkinson divider, a 90° broadside coupler and two unit mixers. The unit mixers employ a drain LO-injection configuration, hence no DC drain bias is required and LO-to-RF-isolation can be attained



(a) Structure



(b) Calculated characteristic impedance and transmission loss

Fig. 5 Structure and calculated results of the TFMS line with a ground slit

using unilateral characteristics of FETs. A multilayer broadside coupler developed in our laboratory is employed to obtain a tight coupling (3dB) in an area as small as 0.1 mm^2 [3]. The Wilkinson divider and 90° hybrid are miniaturized with meander-like TFMS lines.

SINGLE-CHIP TRANSMITTER DESIGN

Figure 6 shows a block diagram of the X-band single-chip transmitter. An IF amplifier, an LO amplifier, an RF amplifier and a balanced upconverter are integrated in a single chip. Figure 7 shows a microphotograph of the fabricated X-band single-chip transmitter. The chip size is only 1.9 × 1.9 mm. Measured conversion gain is better than 20 dB over a very wideband range of 9.5—14 GHz as shown in Fig. 8. The LO suppression ratio, defined as the ratio of LO leak power at RF output port and LO input power, is better than −20 dB for the upconverter and −3 dB for the single-chip transmitter. A third-order intercept point (IP_3) of 15 dBm is achieved, where LO power is 0 dBm and IF frequency is 140 MHz.

In order to minimize the area and to achieve a good balance for the upconversion, the IF amplifier is an RC-coupling 4-stage

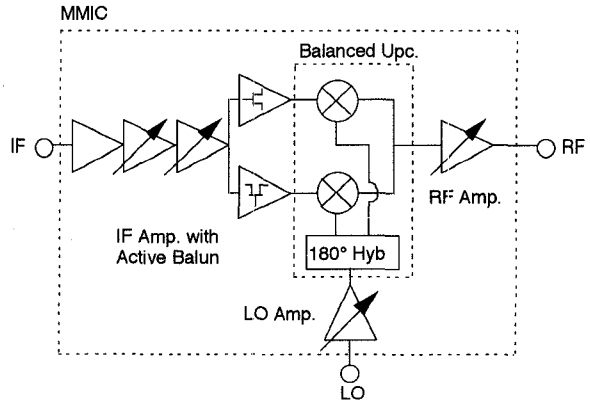


Fig. 6 Block diagram of the proposed 3D MMIC single-chip transmitter which includes a 4-stage IF amplifier with an active balun, an LO amp., an RF amp., two unit mixers and an LO 180° hybrid.

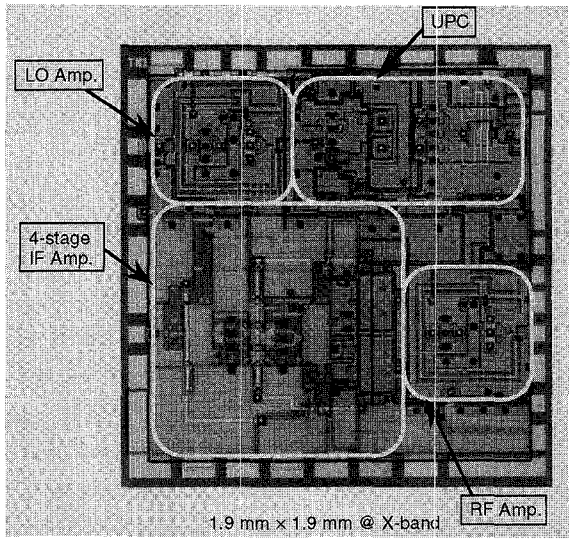


Fig. 7 Microphotograph of the fabricated X-band single-chip transmitter. A 4-stage IF amplifier with an active balun, an LO amp., an RF buffer amp. and a balanced upconverter are integrated in a 1.9 × 1.9 mm chip.

amplifier with the last stage having balanced output ports due to a combination of CGF and CSF, that is, an active balun. The output balance of the IF amplifier is 0.7 dB and 10 degrees at 140 MHz. The IF amplifier is completely covered with the ground metal, therefore, the upper portion of the IF amplifier can be used for other passive circuits. The unit mixers for upconversion employ a gate LO-injection configuration for higher conversion gain, and both are connected at the output ports, in phase.

CONCLUSION

Single-chip X-band receiver and transmitter MMICs which effectively use three-dimensional MMIC technology have been

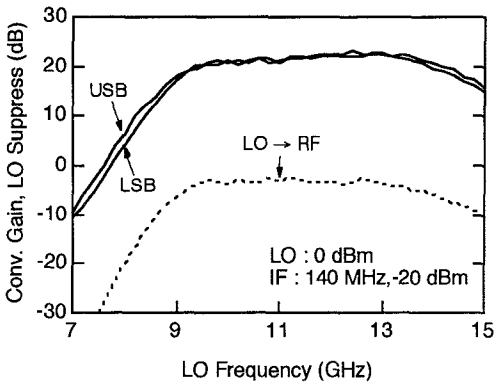


Fig. 8 Measured conversion gain and LO suppression ratio of the fabricated 3D MMIC single-chip transmitter.

demonstrated. Integration level has been significantly increased to a level nearly three times greater than that obtained heretofore. The 3D MMIC technology is a promising tool in the development of highly integrated multifunctional MMICs, and can be effectively applied for many kinds of wireless communication systems.

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